CE-ATA Design Guide

Design Guide ID	**001**
Affected Spec Ver.	**Protocol 1.0**
Corrected Spec Ver.	

Submission info

Name	Company	Date
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Description of design guidance

CE-ATA does not allow another ATA command to be issued while the ATA layer is processing a previously issued ATA command. However, if this situation does occur the device should strive to meet the following objectives with its response:

1. Ensure that there is no data corruption due to this condition.
2. Make the host aware of the error condition.
3. Avoid data driver contention such that there are not issues with transceivers.

Supplemental information

If the device receives a RW_MULTIPLE_REGISTER (CMD60) or a FAST_IO (CMD39) write for the Command register while the ATA state machine is not in state DA_Idle, the device should ensure that there is no data corruption.

Recommended device actions when this condition occurs include either of the following:

1. Return no response to the new MMC command received.
2. Abort the current ATA command and subsequently abort the new ATA command.

Both of these procedures result in the three objectives being satisfied.

Disposition log

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